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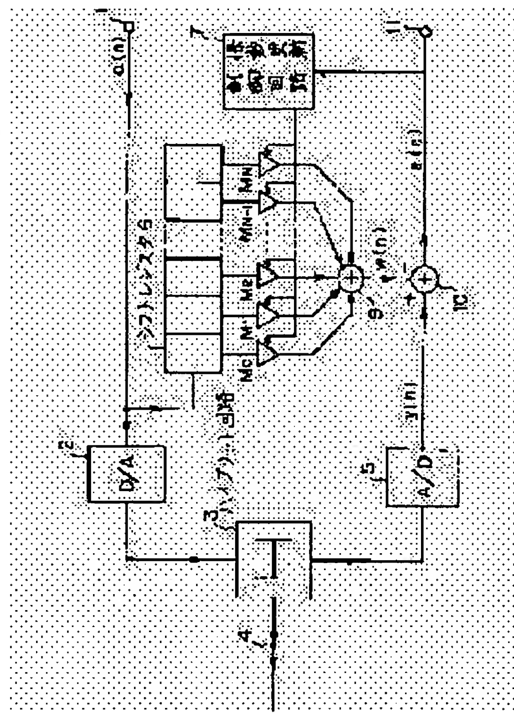
(54) COEFFICIENT CONTROL SYSTEM FOR ECHO CANCELLER



(57)Abstract:

PURPOSE: To make capable of compressing a circuitry for an arithmetic operation by updating a tap coefficient with plural coefficient updation algorithm methods in the echo canceller of transversal filter of a transmitter.

CONSTITUTION: A transmission signal a (n) is inputted to a D/A converter circuit 2 and a shift register 6. The sum of a reception signal and an echo is converted into digital data by an A/D converter circuit 5. An output of each stage of the shift register 6 is fed to multiplier circuits MO-MN, in which the signal is multiplied with a tap coefficient outputted from a coefficient updation control circuit 7 and the result is fed to an adder 9. The coefficient updation control circuit 7 updates a tap coefficient for each cycle by a 1st coefficient updation algorithm after the start of locking. Then each tap coefficient is updated only for once per plural cycles in a 2nd coefficient updation algorithm at least after a lapse of a prescribed time or after a prescribed locking state is reached. The adder 9 adds outputs of the multiplier circuits MO-MN to output a pseudo echo signal w (n).

LEGAL STATUS

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* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the echo canceller of the example of this invention.
[Drawing 2] It is the processing flow chart of the 1st example.
[Drawing 3] It is the processing flow chart of the 2nd example.
[Drawing 4] It is the example Fig. of a solitary-wave response characteristic of an echo.
[Drawing 5] It is the processing flow chart of the conventional echo canceller.
[Description of Notations]
1 11 Terminal
2 D/A Conversion Circuit
3 Yes, Brit Circuit
4 Cable
5 A/D-Conversion Circuit
6 Shift Register
7 Renewal Control Circuit of Multiplier
9 Ten Adder

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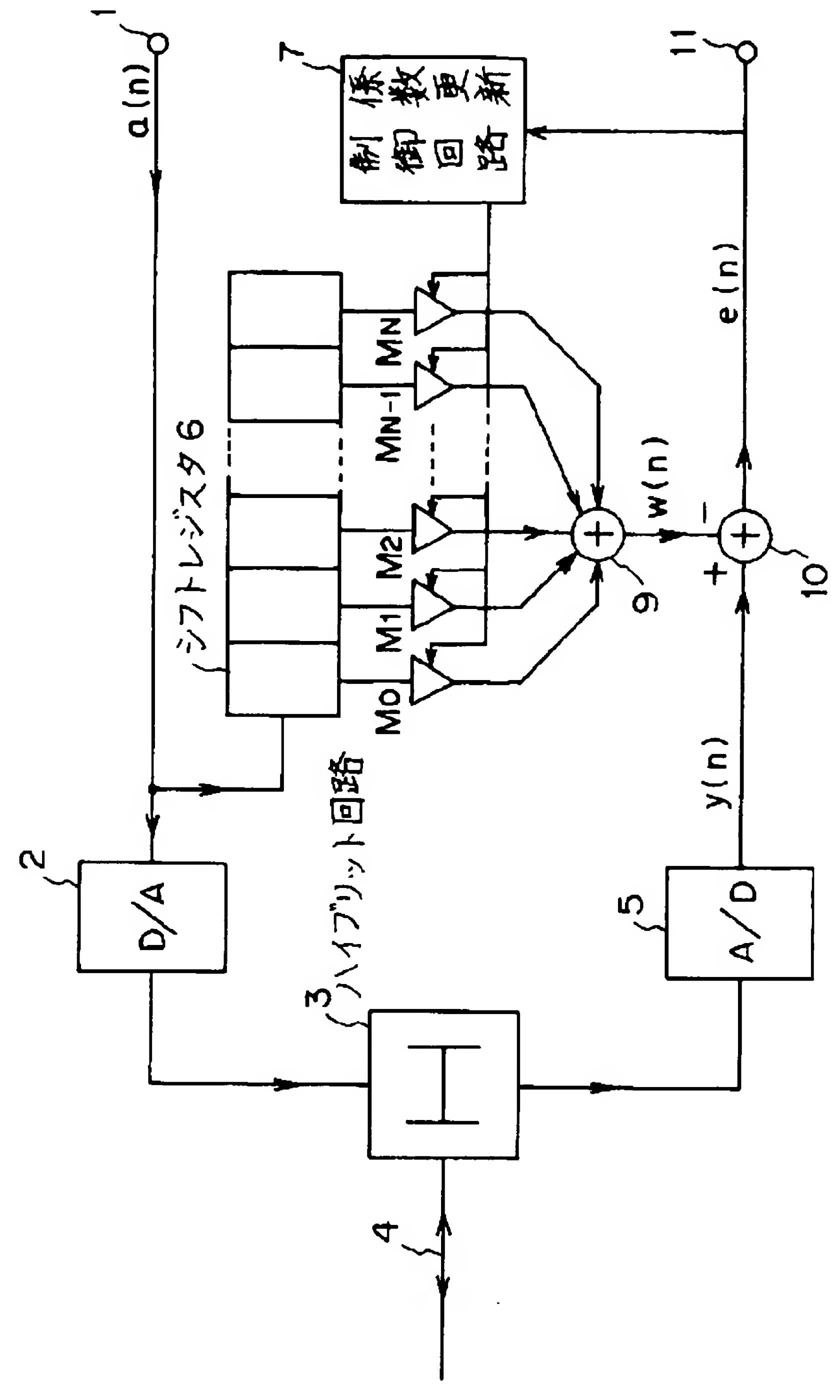
DRAWINGS

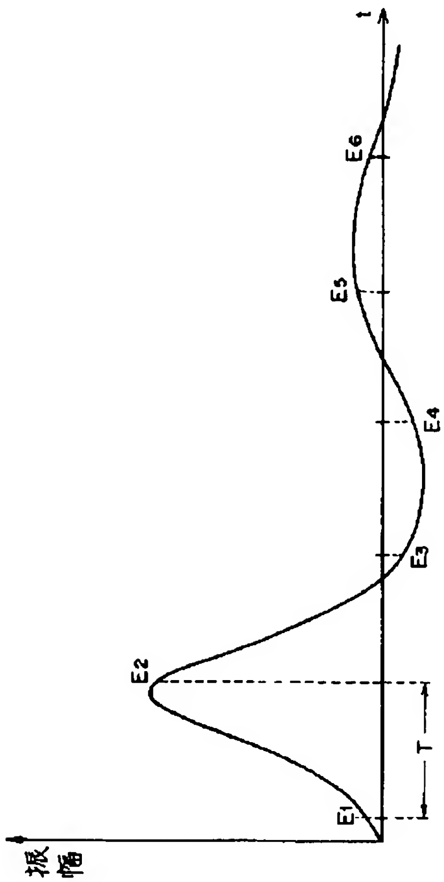
[Drawing 1]

本発明の実施例のエコーキャンセラの構成図



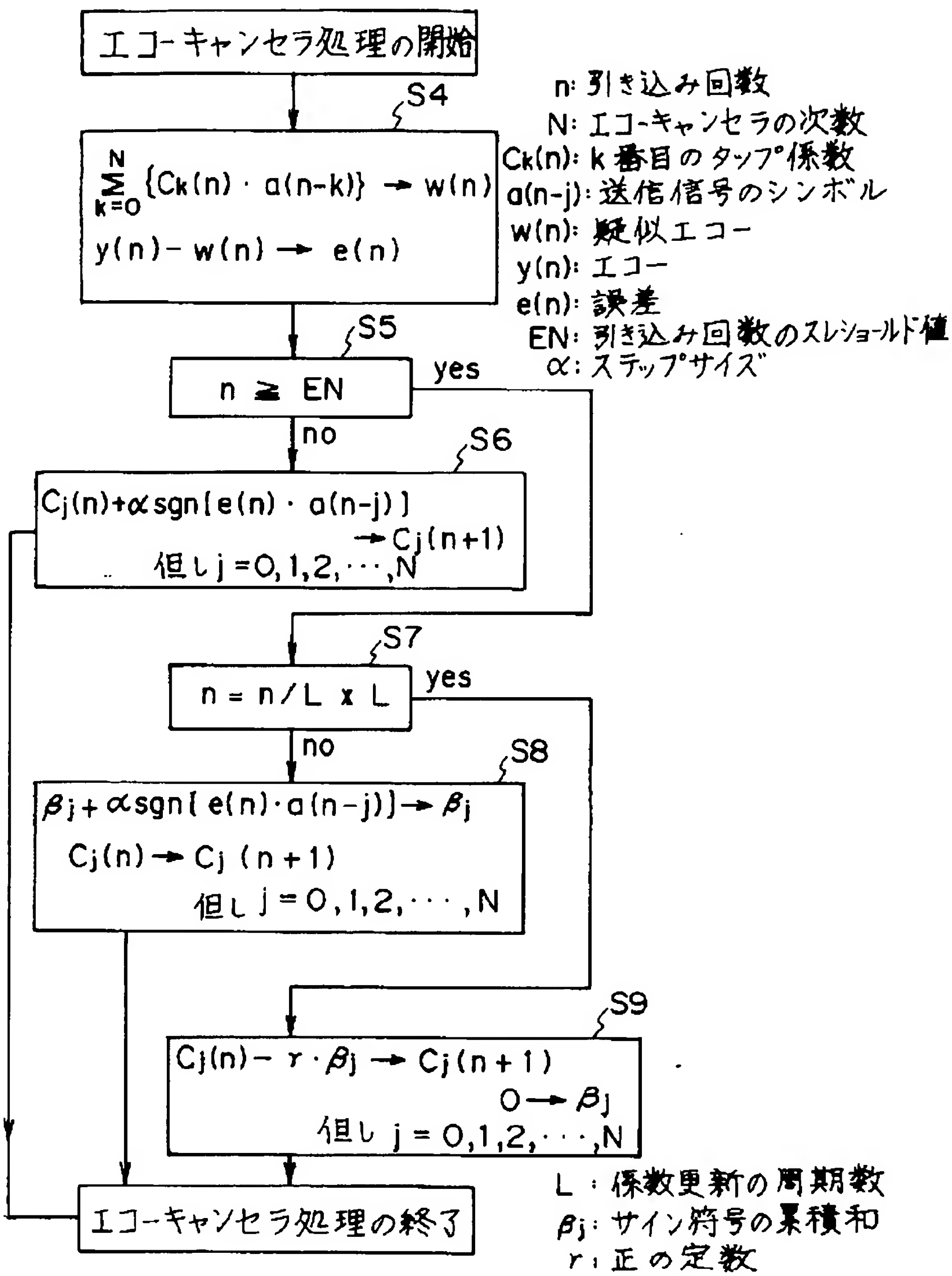
[Drawing 4]

エコーの孤立波応答特性例



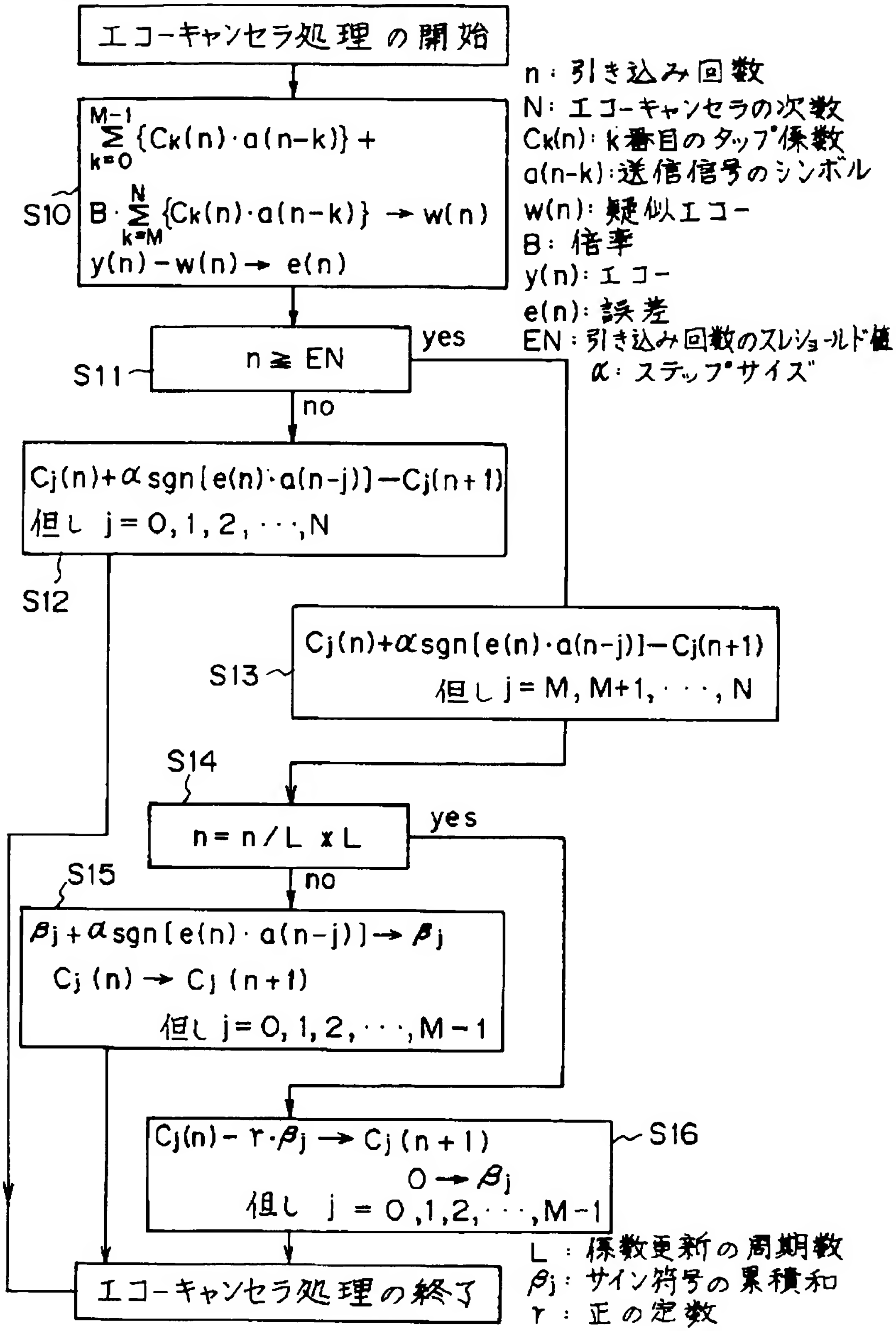
[Drawing 2]

第1の実施例の処理フローチャート



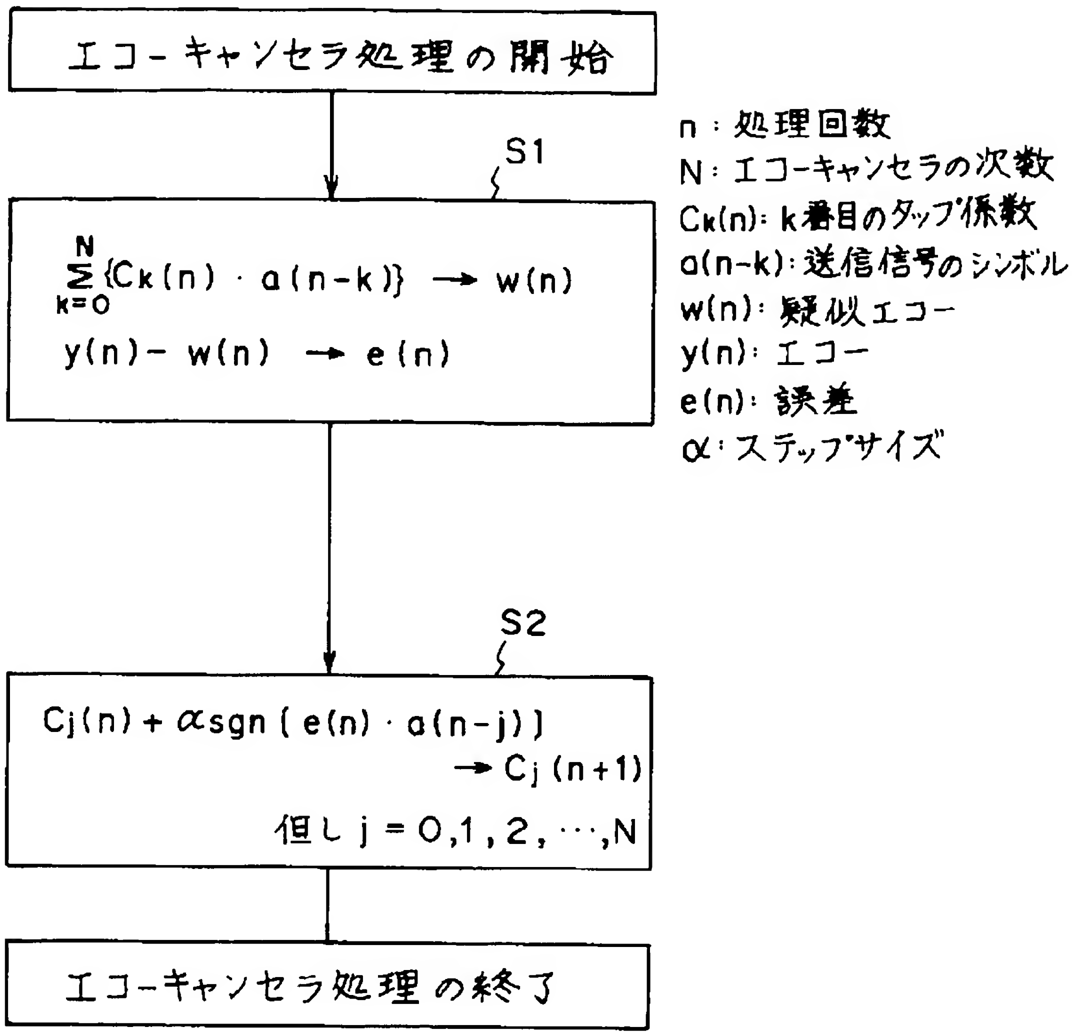
[Drawing 3]

第2の実施例の処理フローチャート



[Drawing 5]

従来のエコーキャンセラの処理フローチャート



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the echo canceller of transmission equipment, and relates to the multiplier control system of the echo canceller which controls the tap multiplier of a transversal filter in more detail.
[0002]
[Description of the Prior Art] In order to transmit high-speed digital data simultaneously to transmission-and-reception both directions using the metallic pair cable of a telephone subscriber line, a digital subscriber line transmission interface device with an echo canceller is required.
[0003] The digital subscriber line transmission interface device using a digital-signal-processing technique is equipment which communicates high-speed digital data using the metallic cable for the existing telephone, and a high speed (80kbaud) and the hybrid equipment which transmits simultaneously the digital data of a multiple value (four values) bidirectionally are used in the equipment. To this hybrid equipment, since it is bidirectional simultaneous transmission, the echo canceller of a transversal filter mold is indispensable.
[0004] Drawing 5 is the processing flow chart of the conventional echo canceller. Processing of drawing 5 is performed in the ** cycle of the clock added to the shift register in a transversal filter.
[0005] When activation is started, it is step S1 and is [0006].
[Equation 1]

$$\sum_{K=0}^{N} \{C_k(n) \cdot (n-k)\}$$

[0007] It is referred to as eye **** and false echo w (n). And the value which lengthened false echo w (n) from sum [of an input signal and an echo] y (n) is set to error e (n). n is a count of processing here.
[0008] Then, it is step S2 and is Cj. (n) + alpha-sgn [e (n) -a (n-j)]
It considers as eye **** and the tap multiplier Cj (n+1) in the following cycle. In addition, alpha is a step size. Step S2 is performed about each tap, and the operation between j= 0 - N is performed.
[0009] Cycle activation of the above-mentioned steps S1 and S2 is carried out sequential [whole]. When the distance of a cable is long, the input signal from a far edge is decreased sharply. On the other hand, a dependence [as opposed to / in a surroundings **** echo / sending signal / via a hybrid circuit / cable distance to a receiving side] is low, and it hardly decreases. for this reason, the amplitude of the echo by the receiving end -- an input signal -- comparing -- +46dB -- namely, -- It may become one 200 times the amplitude of this. Thus, if the amplitude / far-end input signal of an echo are large, it is necessary to attenuate 58dB or more of echoes at least by the echo canceller. The residual echo when attenuating 58dB is set to -12dB to an input signal, and the judgment of an input signal is attained.
[0010] In order to take a digital echo canceller and the surroundings lump magnitude of attenuation of about 60dB, the multiplier word length of the tap multiplier of an echo canceller and the operation word length of the sum-of-products operation of filtering become a problem.
[0011] Usually, although processing of an echo canceller is performed by digital signal processing also including other processings, in order to make hardware into min in that case, it is common to perform the operation by the fixed point system. However, in the case of fixed point arithmetic, since it is influenced by the minimum figure which the precision deals with, it is necessary to examine the multiplier word length well.
[0012] By the operation of the transversal filter of an echo canceller, the long operation word length is required for extent from which the operation word length does not become a problem, and needed for it register 22 bit for a sum-of-products operation, and more than other register 16 bit(s). Moreover, if a tap multiplier is a fixed value, the word length is 16 bits. With extent [more than], the fall of the magnitude of attenuation by the rounding error can be disregarded.

[0013] However, in the case of the echo canceller of a transversal filter mold, processing of the so-called renewal of a multiplier in which only the value equivalent to a step size changes the value of a multiplier based on the multiplication result of the signal symbol and the output error of an echo canceller corresponding to ** cycle each tap is performed, and the multiplier of each tap is not a fixed value. Moreover, the magnitude of a step size is the multiplier word length's least significant. It cannot do smaller than the value equivalent to bit.
[0014] Since a multiplier update process is processing brought close to true value probable, it approaches a true value with blurring in zigzag (i.e., to some extent). When a step size is large, it may become the value from which it separated considerably temporarily from the true purpose value, therefore an error arises, and it stops for this reason, being able to enlarge the surroundings lump magnitude of attenuation.
[0015] Since there is a multiplier update process, in order to obtain the above-mentioned surroundings lump magnitude of attenuation, as for the signal word length, 15 - 16 bit is needed by the conventional echo canceller of 20 to 30 tap for the multiplier word length of the tap multiplier more than 20 bit.
[0016] When updating a tap multiplier, since it is distributed over the range with about 10 times and the becoming breadth of the tap multiplier value ** step size of truth [after / convergence / multiplier / tap], only the value with which a substantial error is equivalent to 3 - 4 bit worsens.
[0017]
[Problem(s) to be Solved by the Invention] As mentioned above, since the formation of 16 bit is difficult, approaches, such as using the special purpose processor which processes all equipments also including other processings in the former by the general-purpose digital-signal-processing processor (DSP) of 20 bit processing, or performs 20 bit processing only for the part of an echo canceller, are performed without it degrades the engine performance about the multiplier word length of the echo canceller of a digital subscriber line transmission interface device.
[0018] 20 When the general-purpose digital-signal-processing processor of bit processing was used, in spite of could manage the processing of those other than echo cancellers, such as a judgment feedback equalizer, with processing of 16 bit, not obtaining the processing fake colander of 20 bit only for the tap multiplier of an echo canceller had the problem which becomes expensive as the whole equipment.
[0019] since an echo canceller and a judgment feedback equalizer generally perform similar processing when it constitutes equipment using exclusive hardware -- tap multiplier bit -- if a number can be held down to 16 bit, it can use to an echo canceller and a judgment feedback equalizer, being able to multiplex one hardware. This has effectiveness in contraction of the scale of the equipment. However, the hardware of dedication had to be conventionally assigned only to the echo canceller like the above-mentioned by 20 bit need, using the hardware of 20 bit in common. For this reason, it had the problem that mitigation of hardware could not be aimed at.
[0020] This invention aims at the multiplier control system of the echo canceller which processes all processings concerning an echo canceller by 16 bits.
[0021]
[Means for Solving the Problem and its Function] This invention can be set to the echo canceller of the transversal filter mold of transmission equipment.
[0022] Since the word length of a tap multiplier is short, if an error stops becoming small even if it updates a ** cycle tap with the 1st renewal algorithm of a multiplier and convergence advances by the 1st configuration until the multiplier word length influences in training processing of an echo canceller, it will update once in two or more cycles at the 2nd process at least by one side after reaching after fixed time amount progress or a fixed drawing-in condition.
[0023] The updating algorithm calculates the product of the error output of a sending-signal symbol value and an echo canceller for every cycle, accumulates only the sign (sign), and makes what deducted the value which multiplied two or more cycles by suitable weight to the accumulation value once from the original tap multiplier a new tap multiplier. This updating can perform highly precise renewal control of a multiplier by the operation of the same number of bits as usual.
[0024] It is seven to 8 tap that the tap multiplier may furthermore become large among the tap multipliers of an echo canceller, about those taps, it controls by the 1st and 2nd above-mentioned process, and updating control by the 1st algorithm is performed about other taps.
[0025]
[Example] Hereafter, this invention is explained to a detail using a drawing. Drawing 1 is the block diagram of the echo canceller used for a digital subscriber line transmission interface device etc. An echo canceller is the Nth transversal filter and is the tap multiplier Cj. It changes accommodative and an echo is negated.
[0026] Sending-signal a (n) is a signal which serves as four values of 3 [**] after [**1] D/A conversion in drawing 1 , and it is usually randomized by the scrambler in false. n presupposes that the time of day of a baud rate unit is

expressed here.
[0027] If sending-signal a (n) is added from a terminal 1, the D/A conversion circuit 2 will change digital sending-signal a (n) into an analog signal. Although the analog signal changed with D/A converter 2 is sent to the other party through a hybrid circuit 3 and a cable 4, an echo comes back for the mismatch between a hybrid circuit 3 and a cable 4. The input signal from a far edge also joins coincidence. This signal is changed into digital data in the A/D-conversion circuit 5. In addition, the sum (digital value) of this input signal and echo is set to y (n) here.
[0028] On the other hand, sending-signal a (n) is inputted into the shift register 6 other than the D/A conversion circuit 2. A shift register 6 is N+1 step of shift register which shifts the data inputted with the same clock as the basic clock of a sending signal. the output of each stage of this shift register 6 -- multiplication circuit M0 -MN the tap multiplier twice which is added and is outputted from the renewal control circuit 7 of a multiplier -- it is carried out and joins an adder 9. Adders 9 are these multiplication circuit M0 -MN(s). An output is added and it outputs as a false echo signal. False echo w (n) which is the output of the transversal filter of an echo canceller is expressed with a degree type.
[0029]
[Equation 2]

$$w(n) = \sum_{K=0}^{N} \{C_k \cdot a(n-k)\} \qquad \cdots\cdots(1)$$

[0030] This false echo w (n) joins an adder 10, and is further added to the sum of the input signal and echo which were changed with A/D converter 5. In addition, since the output of an adder 9 joins the minus (-) terminal of an adder 10, a difference is searched for as a result. This output is remainder e (n) and is e(n) =y(n)-w (n). ...... It is expressed with (2). This remainder e (n) is outputted from a terminal 11 as a received signal.
[0031] The input signal from a far edge is contained in this remainder. Remainder e (n) and sending-signal a (n) is the renewal block of a multiplier, for example, is [0032].
[Equation 3]

$$C_j - \alpha \,\mathrm{sgn}\,[e(n) \cdot a(n-j)] \rightarrow C_j \qquad \cdots\cdots(3)$$

[0033] However, processing of j= 01, ..., N is made and it is the tap multiplier Cj. It changes **alpha every. alpha calls it a step size by the positive number here.
[0034] In order to give qualitative explanation to below, input-signal y (n) is set as follows.
[0035]
[Equation 4]

$$y(n) = R(n) + \sum_{i=0}^{NN} \{E_i \cdot a(n-i)\} \cdots\cdots(4)$$

[0036] R (n) is an input signal from a far edge here. Moreover, Ei It is the amplitude of every cycle of the response characteristic of an echo when only one sending signal is transmitted. An example is shown in drawing 5 . Although this property is also called the solitary-wave response characteristic of an echo, that amplitude does not become quite long cycle zero. (4) Suppose that it continues to NN+1 cycle by the formula.
[0037] Formula (1) (4) (2) It substitutes.
[0038]
[Equation 5]

$$e(n) = R(n) + \sum_{i=0}^{NN} \{E_i \cdot a(n-i)\} - \sum_{k=0}^{N} \{C_k \cdot a(n-k)\} \qquad \cdots\cdots(5)$$

[0039] It is [0040] when a (n-j) is hung on the both sides of this formula.
[Equation 6]

$$e(n) \cdot a(n-j) = R(n) \cdot a(n-j) + \sum_{i=0}^{NN} \{E_i \cdot a(n-i)\} \cdot a(n-j) - \sum_{k=0}^{N} \{C_k \cdot a(n-k)\} \cdot a(n-j) \quad \cdots\cdots (6)$$

[0041] It becomes. Formula (6) If it takes into consideration how it changes over a long cycle about the right-hand side, it will be analyzed as follows. Although input-signal [from a far edge] R (n) is included first, this signal is also randomized by the scrambler in false, and the average of the product of that signal and the sending signal a (n-j) randomized as mentioned above is set to 0 when it sees in a to some extent long period. In addition, random nature is maintained although R (n) has been no longer a discrete signal like **1 and **3 for distortion of a transmission line. Moreover, (6) Since the correlation between the sending signals from which time of day n differs also about the 2nd term of the right-hand side of a formula and the 3rd term is 0, the average of the product is set to 0. Therefore, [0042]
[Equation 7]

$$i = j \qquad k = j \quad \cdots\cdots (7)$$

[0043] About the term of an except, if it sees in a to some extent long period, the probability which becomes negative is the same as the probability which just becomes. It is (6) as mentioned above. Many terms of a formula have the probability which just becomes by itself, and the equal probability which becomes negative, and are the same as the probability for the sum of all terms other than i=j and k=j which add them, and the 1st term to also just become. [of the probability which becomes negative]
[0044] Moreover, (7) About the realized term, it is [0045].
[Equation 8]

$$C_j = E_j \quad \cdots\cdots (8)$$

[0046] Although it becomes **************** 0, in the long run, it is not set to 0 other than it. if it inquires based on the above thing -- (3) a formula -- (6) if a formula is calculated and the sign is forward -- the present tap multiplier Cj from -- if a step size alpha is lengthened and the sign is negative -- the present tap multiplier Cj It means applying the tap size alpha. Therefore, in each cycle, it is the present tap multiplier Cj. Although it sways to positive/negative with the value of input-signal [from a far edge] R (n), and a sending signal, it is the amplitude Ej in the long run. It is influenced and is (8). It converges in the direction in which a formula is realized.
[0047] However, (3) It is made to converge on the amplitude Ej which is a correct answer value gradually probable using the random nature of a signal, and the present tap multiplier Cj drawn from a formula is the present tap multiplier Cj to 1 cycle. Supposing only alpha can change, after convergence may shift to positive/negative both directions to the several times larger value of alpha to a correct answer value in the short term. In such a case, the standard deviation sigma which is an average gap is [0048].
[Equation 9]

$$\sigma^2 = \alpha^2 \, 1/2 + (2\alpha)^2 \, (1/2)^2 + (3\alpha)^2 \, (1/2)^3 + (4\alpha)^2 \, (1/2)^4 + \cdots = 6 \cdot \alpha^2$$

$$\sigma = 2.45 \cdot \alpha \quad \cdots\cdots (9)$$

[0049] ** -- it becomes like. sigma is a coefficient of dispersion here. 3sigma usually considered to be the worst case as a result is set to 7.35 and alpha, will be large by about 3 bit compared with the precision of alpha, and will blur. therefore, a step size -- the time of a fixed tap multiplier -- required min -- bit comparing -- 3 - 4 bit -- it is necessary to make it small because, the maximum of a gap of the multiplier in the case of a fixed tap multiplier -- **1/2 of the minimum precision it is -- since -- it is .

[0050] Since the word length of the tap multiplier decided from a rounding error as a transversal filter becomes 16 bit extent when taking 60dB or more of magnitude of attenuation, alpha becomes the value of 19 - 20 bit precision.
[0051] For this reason, in this invention, after an echo canceller starts drawing in, sufficient time amount passes and an echo canceller changes an algorithm in n>=EN in a quite good drawing-in condition.
[0052] It sets to n>=EN and is a multiplier update process (3) Instead of a formula, it is [0053].
[Equation 10]
n ≠ n／L ＊ L （nがLの整数倍でない）の時

$$\beta_j = \beta_j + \alpha \cdot \mathrm{sgn}\ [e(n) \cdot a(n-j)] \qquad \cdots\cdots(10)$$

[0054]
[Equation 11]

$$C_j \rightarrow C_j \qquad \cdots\cdots(11)$$

[0055]
[Equation 12]
n ＝ n／L ＊ L （nがLの整数倍）の時

$$C_j - \beta_j \cdot \gamma \rightarrow C_j \qquad \cdots\cdots(12)$$

[0056]
[Equation 13]

$$0 \rightarrow \beta_j \qquad \cdots\cdots(13)$$

[0057] ****** is performed. L is a larger integer than 2 here, it is usually about 32 to 64 value, and gamma is a quite small positive number compared with 1 like 0.25. alpha is a step size and is the minimum value allowed from the precision of a multiplier.
[0058] (10) By processing of - (13) type, it is betaj at the time of n!=n/L*L. (6) It becomes what hung alpha on the polar accumulation value of a formula. Of course, it is betaj at n=n/L*L. It is cleared. Moreover, a tap multiplier is fixed between n!=n/L*L. And it is betaj if it becomes that of n=n/nL*L. Only the value which hung the proportionality constant gamma updates a tap multiplier.
[0059] Drawing 2 is the flow chart of the 1st above-mentioned example. It performs, whenever a shift register 6 shifts sending-signal a (n). Initiation of activation asks for false echo w (n) and error e (n) by step S4. This step S4 is the same as that of the conventional step S1. In addition, this is the adders 9 and 10 in drawing 1 , and multiplier M0 -MN. It asks.
[0060] Then, it asks for whether n is more than EN at step S5. (NO) and when [if it puts in another way,] n is not more than EN, and n will be under En, the renewal control circuit 7 of a multiplier asks for the tap multiplier corresponding to each tap at step S6. This step S6 is the same as the conventional step S2. And after step S6 ends the processing corresponding to the clock of drawing 1 . When n is under EN, it becomes the same processing as usual.
[0061] On the other hand, when n distinguishes more than from EN at step S5, it distinguishes whether n=n/L*L is realized at step S7. This formula is a formula from which n distinguishes whether it is the integral multiple of L, and this formula is materialized when it is an integral multiple.
[0062] When it is not an integral multiple, step S8 is performed to (NO), and the value of alpha-sgn [e (n) -a (n-j)] is accumulated. Namely, Bj+ alpha-sgn Bj treating [e (n) -a (n-j)] Processing to store is performed. And it is Cj about Cj (n+1). It is referred to as (n). This means not changing a tap multiplier. This is performed by 0 - N tap, and while ending step S8, the processing corresponding to 1 time of a clock is ended.
[0063] moreover, Bj accumulated until now when n was the integral multiple of L (YES) gamma twice (forward constant) -- carrying out -- the value -- tap multiplier Cj the value lengthened from (n) -- the following tap multiplier Cj (n+1) -- carrying out -- further -- Bj It clears. In addition, this processing is performed by 0 - N tap.
[0064] After step S9 ends the processing corresponding to the clock of drawing 1 . The above actuation is performed one by one corresponding to a clock. At this time, a tap multiplier becomes modification once at L times.
[0065] Taking the case of the case of L= 48 and gamma= 0.25, (10) types are considered now. From the above-mentioned examination result to the case of being close to the worst case of 3sigma is assumed, and it is [0066].

[Equation 14]

$$7.35 \cdot \alpha > \beta_j > -7.35 \cdot \alpha$$

$$1.84 \cdot \alpha > \beta_j \cdot \gamma > -1.84 \cdot \alpha \qquad \cdots\cdots(14)$$

[0067] It becomes. When a multiplier is 16 bit precision, it is shown that only an amount with the tap multiplier near the value corresponding to the minimum precision of worst 15 bit precision may change.
[0068] Consequently, when all processings are conventionally processed by 16 bit, having changed to zigzag to one 8 times the magnitude of a step size with the worst case is settled in 2 double less or equal with the worst case, and degradation of the surroundings lump magnitude of attenuation also decreases.
[0069] As mentioned above, by introducing processing in which an average is taken over L cycle, this invention can make small blurring of the zigzag nature produced for probable processing, while the step size has been large. However, since a tap multiplier is updated only once in L cycle, the rate of updating becomes slow compared with the conventional case. However, in the case of the phase [of having already drawn mostly and the tap multiplier having become the immediately near value of the target value, and the rest making a step size small, bringing it close to a precision more, and enlarging the surroundings lump magnitude of attenuation more], the rate is not a problem.
[0070] Although it assumes carrying out processing of (10) - (13) to all tap multipliers in the example 1, it is also possible to carry out only to some tap multipliers. In addition, these processings are parameter betaj although especially the throughput does not increase compared with the conventional tap multiplier update process. Required memory increases by installation.
[0071] In order to prevent the increment in this memory, in the 2nd example, only about the tap which may become large [a tap multiplier], (10) - (13) is processed and that step size is enlarged [multiplier / of other taps] by updating a multiplier, for example to a true multiplier 8 times the value of a tap.
[0072] Although the solitary-wave response characteristic of the echo which shows an example to drawing 4 changes the form by the existence of the die length of a cable, a class, and a branch cable etc., in any cases, the thing with the large amplitude is up to seven to 8 tap. It is the maximum of the tap multiplier so far **1.0 When it carries out, the tap multiplier after it is **1/8. It becomes below.
[0073] Drawing 3 is the flow chart of the 2nd example of this invention. Although it will ask for false echo w (n) at step S10 if processing is started as mentioned above, the operation at this time uses (15) types. And the value which lengthened false echo w (n) from echo y (n) is set to error e (n).
[0074] Then, it asks for whether n is more than EN at step S11. When n is not more than EN, the renewal control circuit 7 of a multiplier asks (NO) for the tap multiplier corresponding to each tap at step S12. And after step S12 ends the processing corresponding to the clock of drawing.
[0075] On the other hand, when n is more than EN, a tap number is a tap multiplier from M to N at step S13 (3) It considers as the same value as a formula. And when not being distinguished and materialized [whether it is n=n/L*L and] at step S14, while a tap number makes the tap multipliers from 0 to M-1 at (NO) the same as an old value, it is Bj (the result of having added e (n) -a (n-j)] is set to Bj.). Alpha-sgn And processing is ended. Moreover, when n=n/L*L is materialized at step S14, it is Cj (n+1) at step S16 C3 - Gamma-betaj It carries out and is betaj further. Processing set to 0 is performed. However, J is between zero to M-1, and is accumulation sum betaj of the tap multiplier Cj (n+1) in the meantime and a sign sign. It updates.
[0076] Although drawing 3 shows the flow chart of the 2nd example Here about the tap to zero to M-1 (10) Process - (13), and about M tap or subsequent ones, noting that tap multiplier xB (B< 1) is a true tap multiplier At the time of the sum-of-products processing which asks for the output of the transversal filter of an echo canceller, as shown in (15) types, B is hung to the sum-of-products value after M tap. thus -- if it carries out -- multiplier Ck after M tap B-Ck which is a true tap multiplier when the same alpha as the former is used to the value, since it becomes 1/B time and a big value compared with the conventional case It receives and alpha-B becomes a step size equivalent. For example, B=1/8 By carrying out, it is a substantial step size One eighth Degradation of the surroundings lump magnitude of attenuation which is made, therefore is produced harder [which is probable processing] can be made small.
[0077]
[Equation 15]

$$w(n)' = \sum_{k=0}^{M-1} \{C_k \cdot a(n-k)\}$$

$$+ B \cdot \sum_{k=M}^{N} \{C_k \cdot a(n-k)\} \quad \cdots\cdots(15)$$

[0078] In addition, although it came by explanation of the above this invention about all renewal of a multiplier for being a sign algorithm, it is (3) in fact. The processing which removed sign processing in formulas, such as (10), is also possible. Moreover, the 1st process of this invention may be divided into two more sub processes, processing which removed sign processing at the first process may be performed, and a sign algorithm may be carried out at a next process. This invention is effective also to such a case, and also when there is no sign sign, it cannot be overemphasized that it is contained in the generic claim of this invention.
[0079]
[Effect of the Invention] Since what lengthened the multiplier word length of an echo canceller, therefore a signal-processing part for example, with 20 bit conventionally by applying this invention can be shortened like for example, 16 bit, not only memory but an arithmetic circuit is effective in the circuit scale being compressible.
[0080] Furthermore, it is low. If bit processing is attained, since processing speed can be gathered, it is effective in the design of hardware becoming easy. Furthermore, since 16 bit processing is attained, it becomes possible to constitute a digital subscriber line transmission interface device by the general-purpose digital-signal-processing processor.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] The multiplier control system of the echo canceller characterized by consisting of the 2nd process which updates each tap multiplier only once in two or more cycles with the 2nd renewal algorithm of a multiplier with the 1st renewal algorithm of a multiplier after drawing-in initiation in the echo canceller of the transversal filter mold of transmission equipment at least by one side after reaching the 1st process which updates a ** cycle multiplier, and after fixed time amount progress or a fixed drawing-in condition.
[Claim 2] Said 1st renewal algorithm of a multiplier is the multiplier control system of the echo canceller according to claim 1 characterized by changing by the specific value corresponding to the updating sign which is the sign of the multiplication result of the signal and the output error of an echo canceller which correspond about each tap.
[Claim 3] Said 2nd renewal algorithm of a multiplier is the multiplier control system of the echo canceller according to claim 2 characterized by being what deducts from the original multiplier what added said updating sign over two or more cycles about each tap, and multiplied the result by weight.
[Claim 4] It is the multiplier control system of the echo canceller according to claim 1 characterized by performing said 1st and 2nd process only about the tap which may become beyond the value which has the absolute value of the tap multiplier value among the taps of the echo canceller of transmission equipment, and updating a cycle tap multiplier the whole twist to said 1st renewal algorithm of a multiplier about other taps.

[Translation done.]